AN88161(AN/AF/AS/AT)

16-Bit Constant current LED driver with 3.0V to 5.5V supply voltage

Description

The AN88161 is a 16-Bit constant current LED driver IC which is designed for LED displays. The output current can be adjusted by using an external resistor. All outputs will have the same current drive level which is crucial in LED display application. This driver has built-in 16-bit constant current outputs, a 16-bit shift register, and a 16-bit latch circuit. These drivers have been designed by using a HV-CMOS process.

Feature

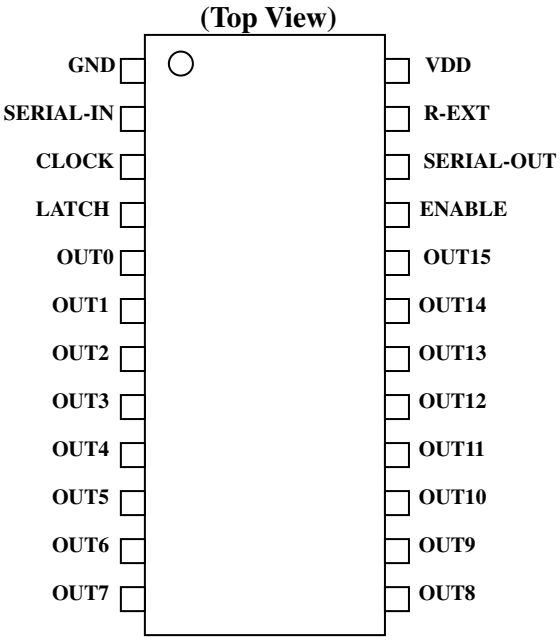
*Output current capability: 90mA each output
*Constant current range: 5mA to 90mA
*For common anode LED application
*Power supply voltage range VDD=3.0 to 5.5V
*Maximum output drain voltage exceeds 17V
*Serial data transfer rate: 25Mhz(Cascade Connection)
*Operating temperature range: -40 to 85 degrees
*Current accuracy:

Between Bits : < +-6 %
Between ICs: < +-10%

*Order information:

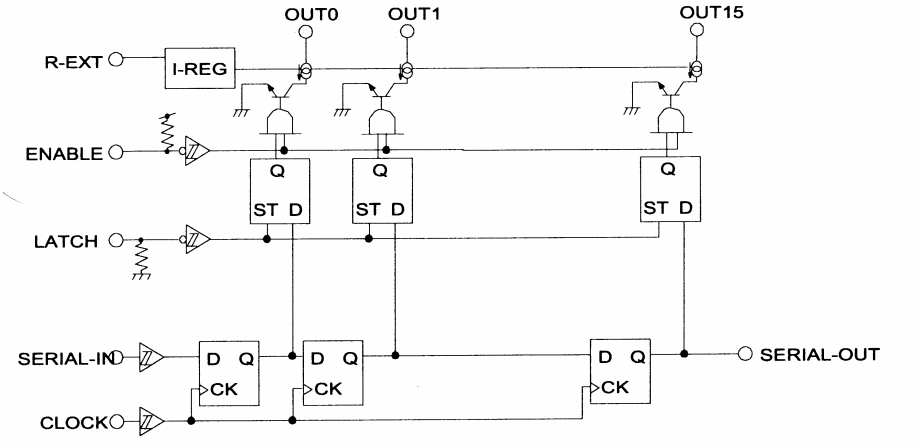
AN88161AN ------ 24SDIP(300mil)
AN88161AF ------- 24SSOP(300mil, 1.0mm lead-pitch)
AN88161AS ------- 24SOP(300mil, 1.27mm lead-pitch)
AN88161AT ------- 24SSOP(150mil, 0.64mm lead-pitch)

Pin Assignment



Do not short circuit the output terminal (OUT0 ~ OUT15) to VDD it will damage the device.

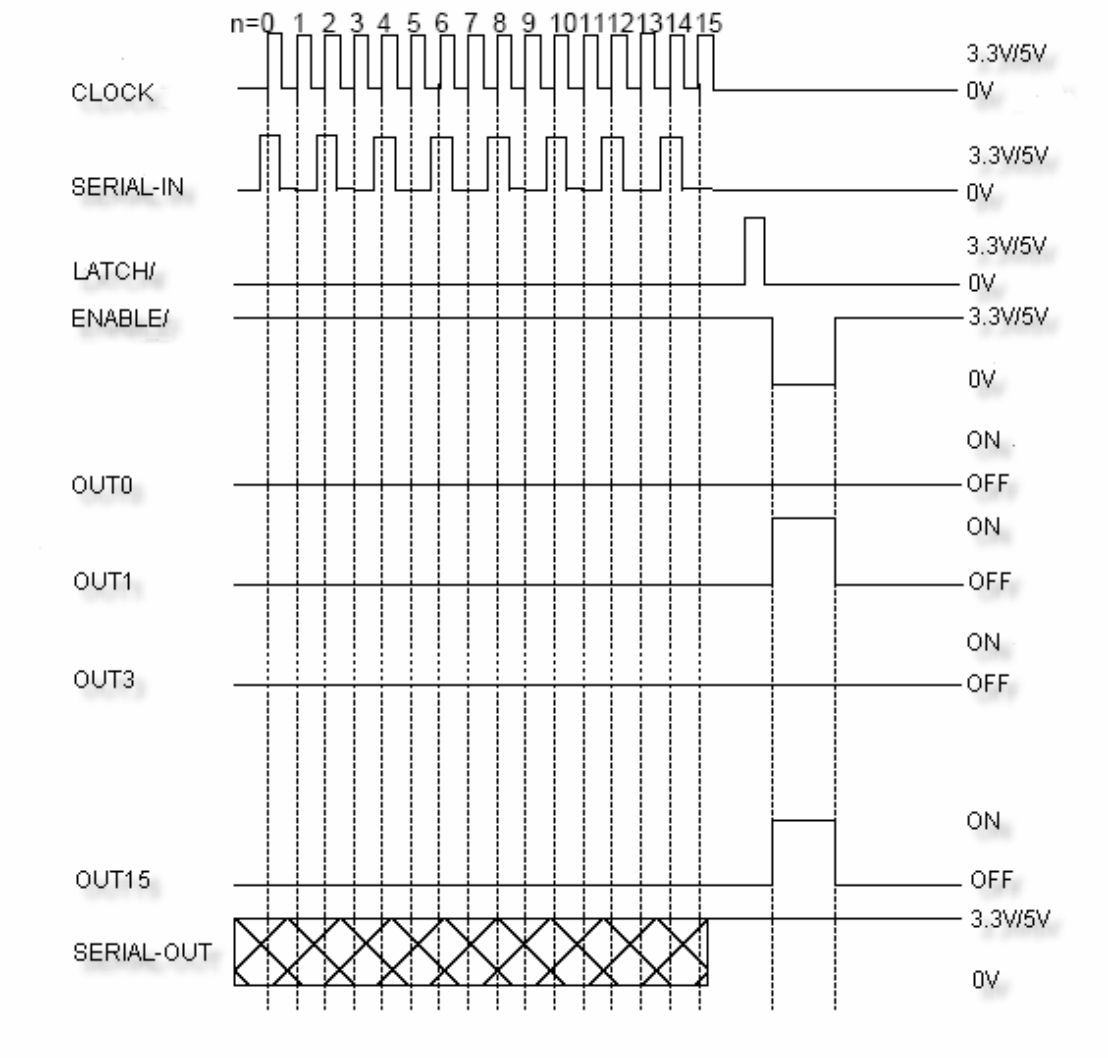
Block Diagram



Truth Table

CLOCK	LATCH	ENABLE	SERIAL-IN	OUT0---OUT7---OUT15	SERIAL-OUT
Positive edge	H	L	Dn	Dn---Dn-7---Dn-15	Dn-15
Positive edge	L	L	Dn+1	No Change	Dn-14
Positive edge	H	L	Dn+2	Dn+2---Dn-5---Dn-13	Dn-13
Negative edge	X	L	Dn+3	Dn+2---Dn-5---Dn-13	Dn-13
Negative edge	X	H	Dn+3	Off	Dn-13

Timing Diagram



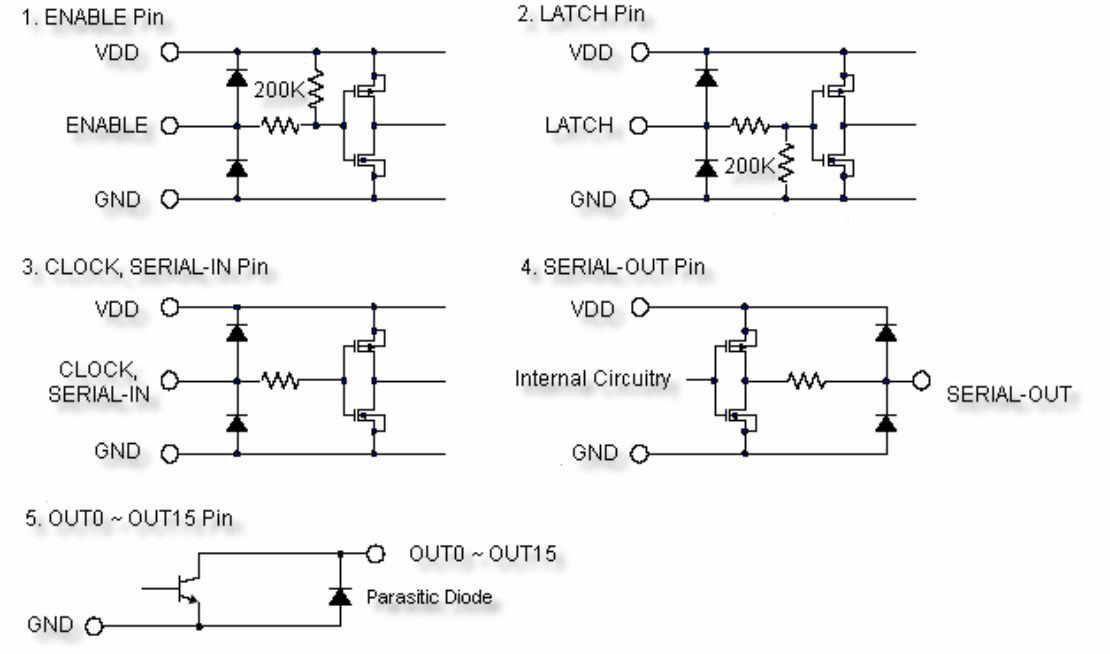
Note:

1. The latch circuit is a level-latch, not a edge-triggered latch.
2. The latch circuit holds data when LATCH pin low, when the LATCH pin is at high-level the latch circuit passes the data from input to output. When ENABLE pin is at low-level, the latch is data transferred to the output pin OUT0~OUT15.
   When ENABLE pin is at high-level, the OUT0~OUT15 is turned off regardless of the latch data.

Pin Description

Pin o.	Pin Name	Function
1	GND	GND Pin
2	SERIAL-IN	Serial input data pin
3	CLOCK	Clock input terminal for shift register, rising edge trigger
4	LATCH	Data latch input pin. When LATCH=High-level, data is passed to OUT0~OUT15, when LATCH=Low-level, data is latched.
5~20	OUT0~OUT15	16 constant current output pin to drive common anode LEDs
21	ENABLE	Data output enable pin, when ENABLE=High-level, all OUT0~OUT15 are turned off, and when ENABLE=Low-level, all OUT0~OUT15 are enabled.
22	SERIAL-OUT	Serial data output pin for cascade operation
23	R-EXT	The external resistor connection pin to adjust the output current
24	VDD	3.3V~5.5V supply voltage pin

Equivalent circuits of I/O pins



Absolute Maximum Ratings

Characteristics	Symbol	Rating	Unit
Supply Voltage	VDD	+7	V
Input Voltage	Vin	-0.4 to VDD+0.4	V
Output Current	Iout	+90	Ma
Output Voltage	Vout	-05 to 20	V
GND Pin current	IGND	1920	mA
Clock Frequency	fCLK	25	Mhz
Power Dissipation	Pd	AN: 2.87 AF: 1.45 AS: 1.45	W
Thermal Resistance	Rth(j-a)	AN: 40 AF: 79 AS: 79	℃/W
Operating Temperature	Top	-40 to 85	℃
Storage Temperature	Tstg	-55 to 150	℃

Recommended Operating Condition

Characteristics	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage	VDD		3	5	5.5	V
Output Voltage	VOUT				30	V
Output Current	IOUT IOL IOH	OUTn SERIAL-OUT Vol=0.7V Voh=4.3V			90 2.5 -3.0	mA
Input Voltage	VIL VIH		0.7VDD -0.3		VDD+0.3 0.3VDD	V
Clock Frequency	fCLK	VDD=5V, Cascade connection VDD=3V, Cascade connection			25 20	Mhz
Latch Pulse Width	twLatch	VDD= 4.5V ~ 5.5V	15			ns
Clock Pulse Width	twCLOCK	VDD=4.5V ~ 5.5V	15			ns
Set-up Time for Data	tSETUP 3	VDD=4.5V ~ 5.5V	20			ns
Set-up Time for Latch	tSETUP 2	VDD=4.5V ~ 5.5V	15			ns
Set-up Time for Clock	tSETUP 1	VDD=4.5V ~ 5.5V	20			ns
Hold Time for Data	tHOLD	VDD=4.5V ~ 5.5V	20			ns

Electrical Characteristics(Temp=25℃)

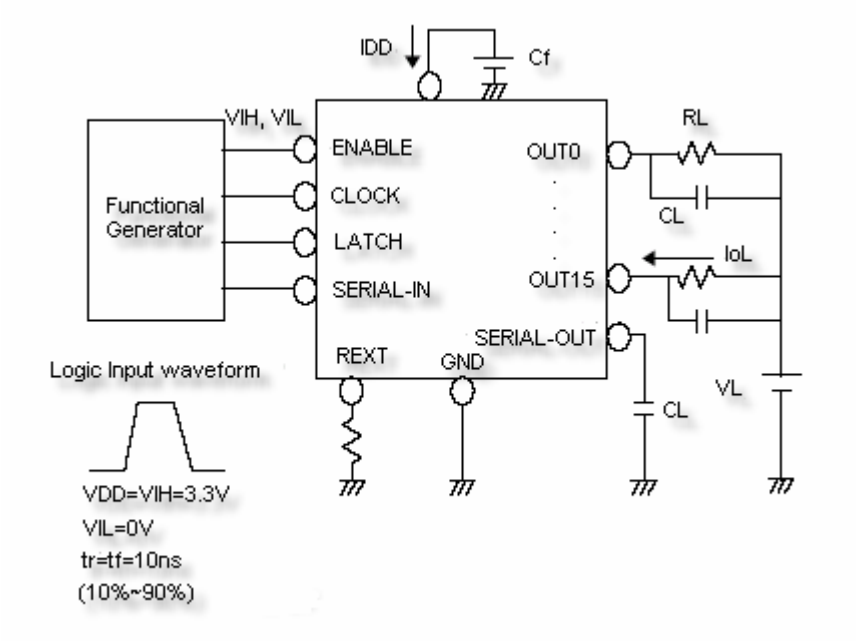
Characteristics	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage	VDD		3		5.5	V
Output Current	IOUT1	VOUT=0.7V, VDD=3.3V, R-EXT=499Ohm		34		mA
	IOUT2	VOUT=0.7V, VDD=5.0V, R-EXT=499Ohm		34		
	IOUT3	VOUT=0.7V, VDD=3.3V, R-EXT=200Ohm		81		
	IOUT4	VOUT=0.7V, VDD=5.0V, R-EXT=200Ohm		81		
Output Current Error	IOUT1	VOUT=0.7V, R-EXT=499Ohm	2		4	%
Between Bits	IOUT2	VOUT=0.7V, R-EXT=200Ohm	2		6	
Output Current Error	ILO3	VOUT=0.7V, R-EXT=499Ohm	8		10	%
Between Chip	IOL4	VOUT=0.7V, R-EXT=200Ohm	10		12	
Output Leakage Current	ILEAK	VOUT=25V			1	uA
Input Voltage Low	VIL	VDD=5V	0		1.5	V
Input Voltage High	VIH	VDD=5V	3.5		5.0	V
Output Voltage SOUT	VOL	IOL=+2.5mA, VDD=3.3V			0.3	V
		IOL=+2.5mA, VDD=5V			0.4	
		IOL=-2.5mA, VDD=3.3V	2.7			
		IOL=-2.5mA, VDD=5V	4.6			
Pull-up Resistor	R(UP)	ENABLE Pin		200		K
Pull-down Resistor	R(DOWN	LATCH Pin		200		K
Supply Current(Off)	IDD(Off)	VDD=5.0V, R-EXT=499Ohm		5.2		mA
(OUT0~OUT15 Off)		VDD=5.0V, R-EXT=200Ohm		12.5		
		VDD=3.3V, R-EXT=499Ohm		5.0		
		VDD=3.3V, R-EXT=200Ohm		12.4		

Switching Characteristics(Temp=25℃,VDD=VIH= 5V, VIL=0V,R-EXT=470Ohm)

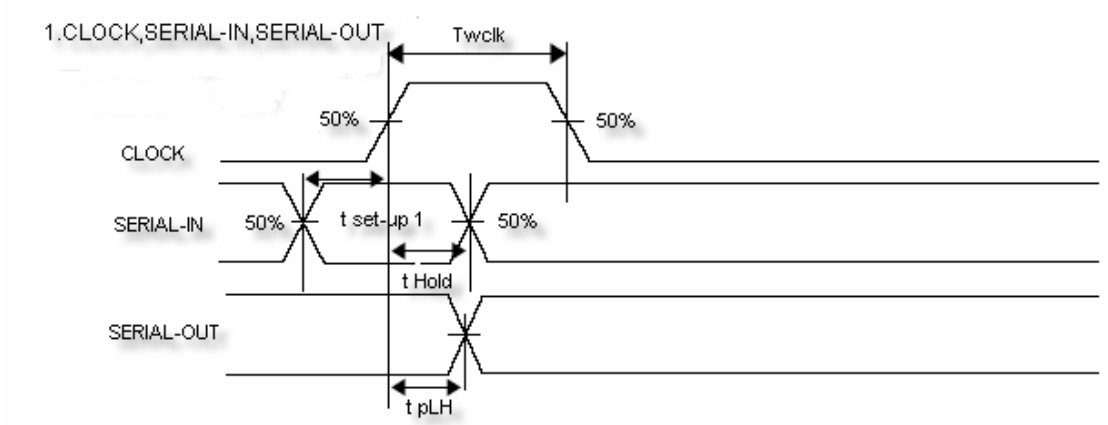
Characteristics	Symbol	Condition	Min	Typical	Max	Unit
Propagation Delay	tpLH1	CLK-OUTn, LATCH="H",ENABLE="L"	35			ns
	tpLH2	LATCH-OUTn, ENABLE="L"	20			ns
	tpLH3	ENABLE-OUTn, LATCH="H"	30			ns
	tpLH	CLK-SERIAL OUT	15			ns
	tpHL1	CLK-OUTn,LATCH="H", ENABLE="L"	35			ns
	tpHL2	LATCH-OUTn,ENABLE="L"	20			ns
	tpHL3	ENABLE-OUTn,LATCH="H"	30			ns
	tpHL	CLK-SERIAL OUT	15			ns
Output rise time	tor	Voltage waveform 10%~90%	30	75	150	ns
Output fall time	tof	Voltage waveform 90%~10%	10	20	40	ns
Max CLK rise time	tr				5	ns
Max CLK fall time	tf				5	ns

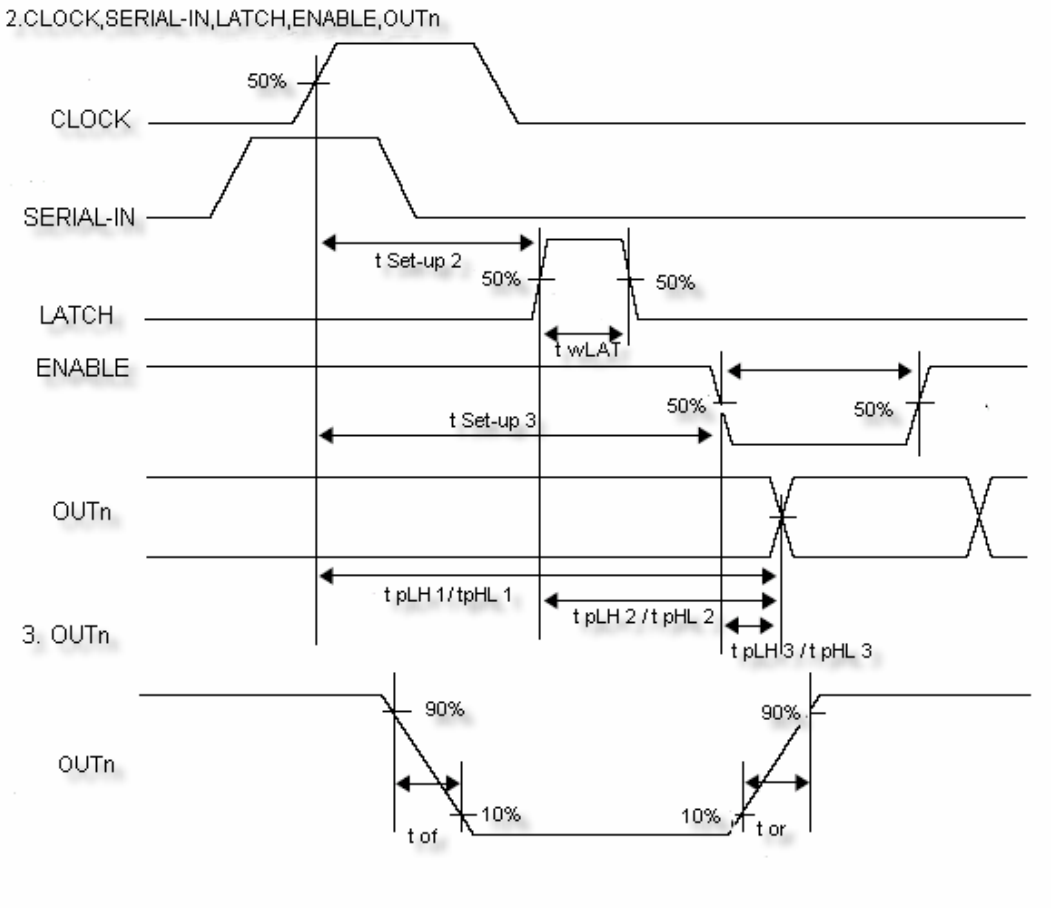
Test circuit

(RL=65Ohm, CL=13pf, VL=3.0V)



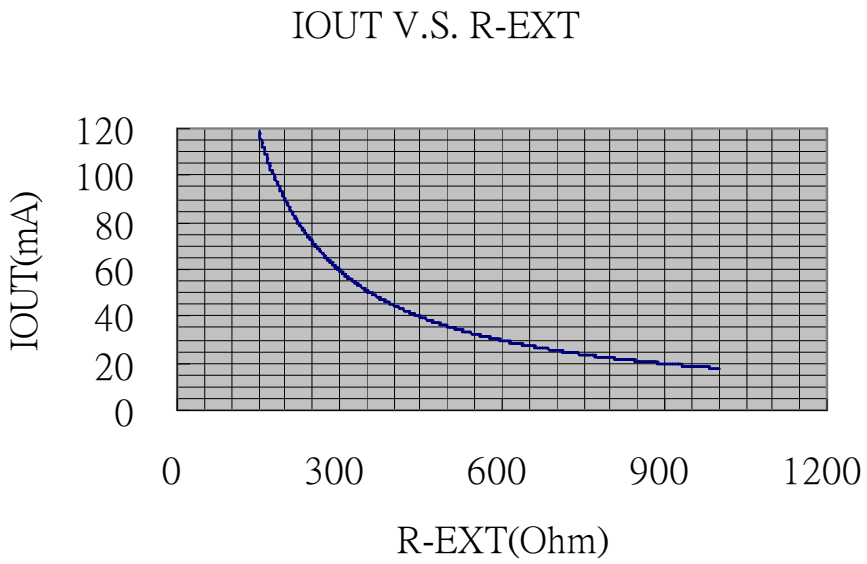
Timing Waveform



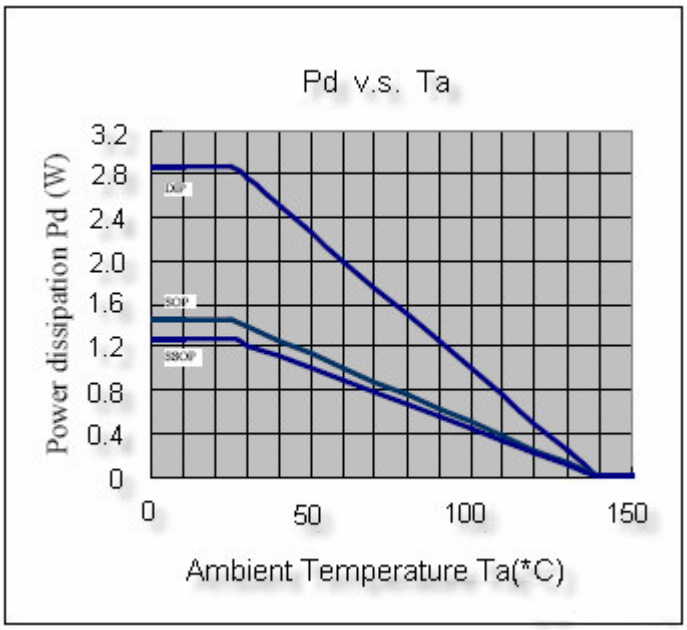


Output Current V.S R-EXT(VDD=5V)

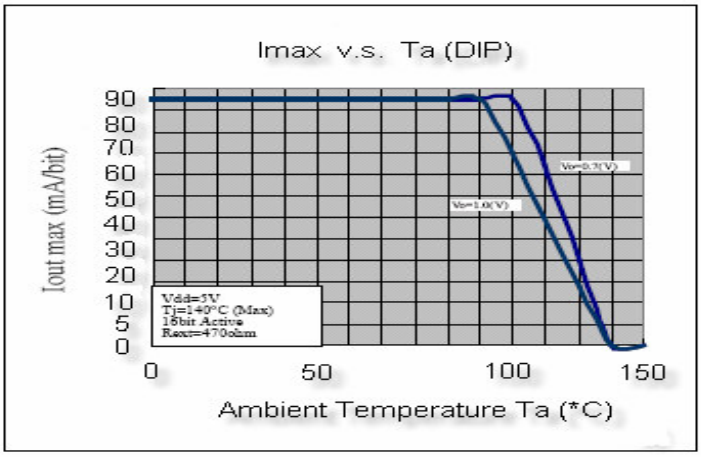
Iout = Vref/Rext * 14.23

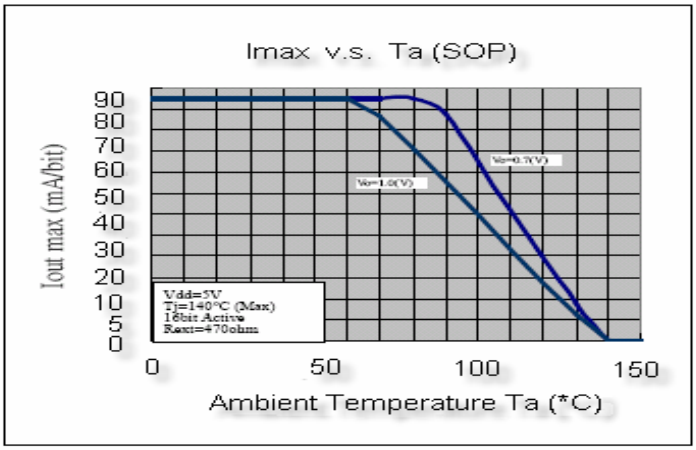


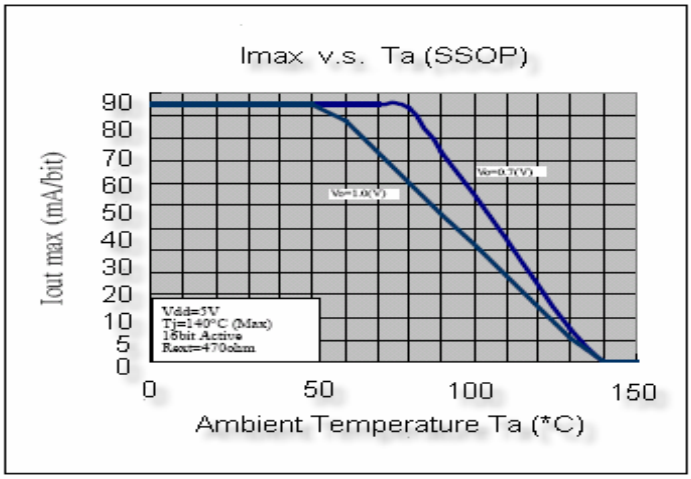
Package Power Dissipation



I out v.s. Ta


Imax v.s. Ta (DIP)
Iout max (mA/bit)
90
80
70
60
50
40
30
20
10
5
0
Vdd=5V
Tj=140°C (Max)
16bit Active
Rext=470ohm
0
50
100
150
Ambient Temperature Ta (*C)


Imax v.s. Ta (SOP)
Iout max (mA/bit)
90
80
70
60
50
40
30
20
10
5
0
Vdd=5V
Tj=140°C (Max)
16bit Active
Rext=470ohm
0
50
100
150
Ambient Temperature Ta (*C)


Imax v.s. Ta (SSOP)
Iout max (mA/bit)
90
80
70
60
50
40
30
20
10
5
0
Vdd=5V
Tj=140°C (Max)
16bit Active
Rext=470ohm
0
50
100
150
Ambient Temperature Ta (*C)

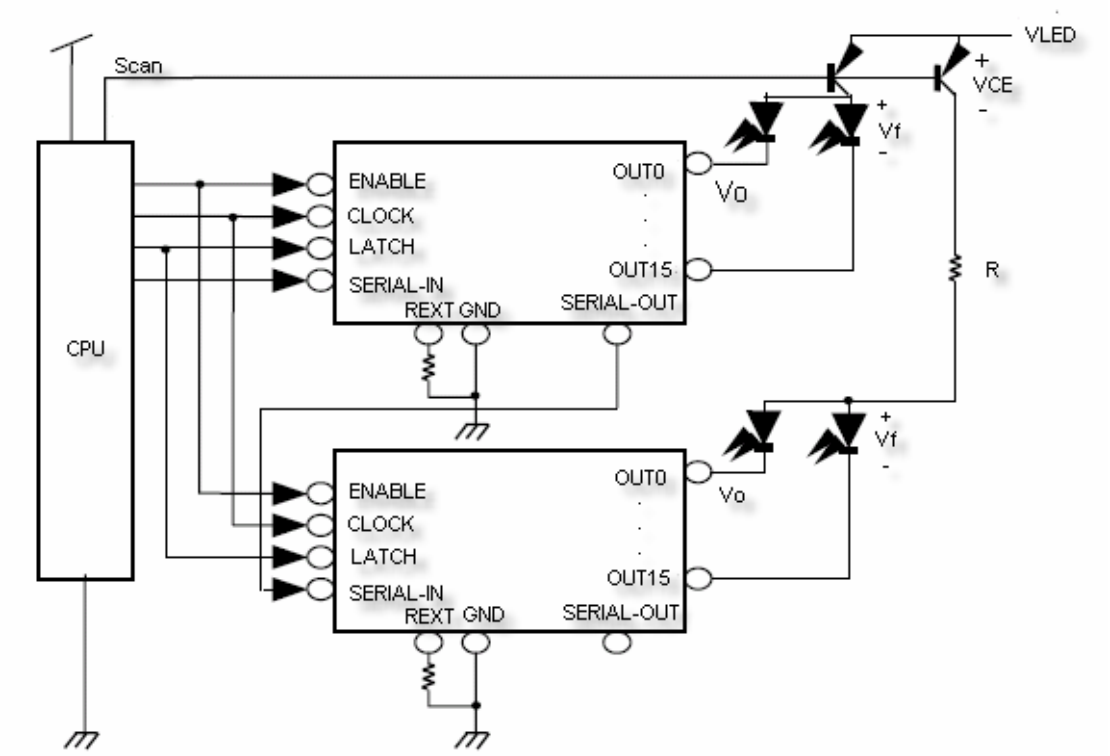
Typical Application

LED supply voltage is set-up by following equation:

$V_{LED} = V_{CE} + Vf + Vo$

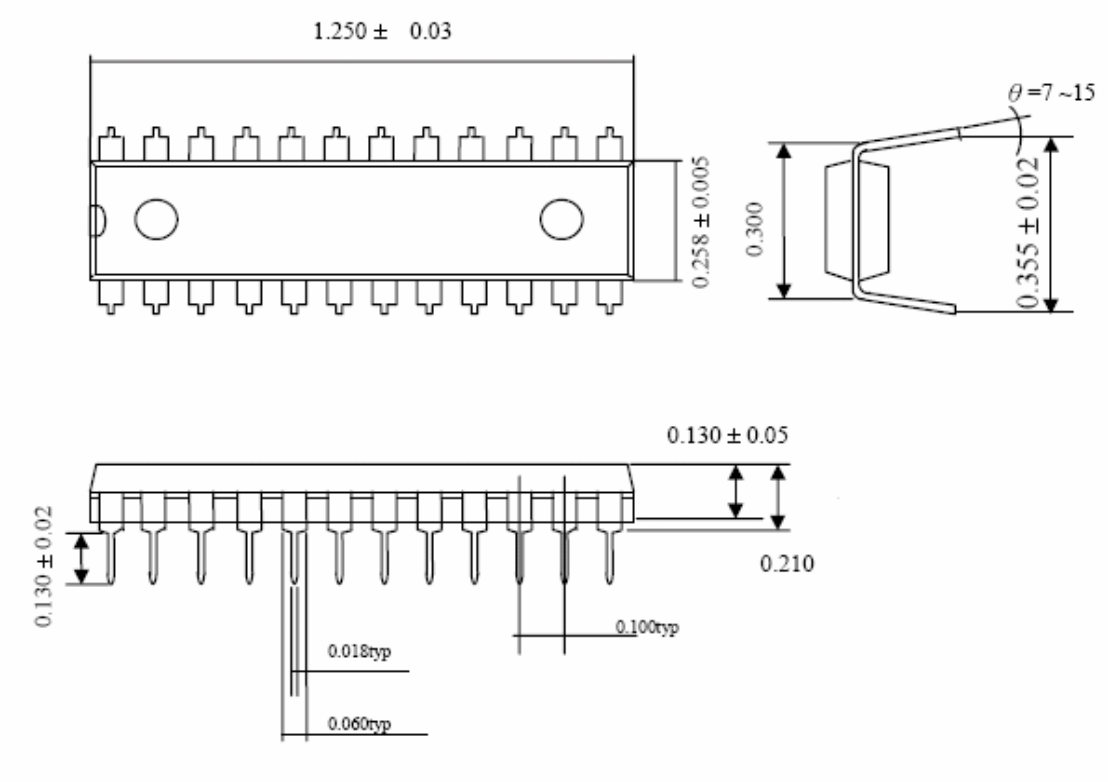
To prevent too much power dissipated by driver due to the higher V_{LED}, an additional R can be introduced to reduce the Vo when output is consuming current.

$R = (V_{LED} – V_{CE} – Vf – Vo\ min)/ (Io\ max * Bit\ max)$



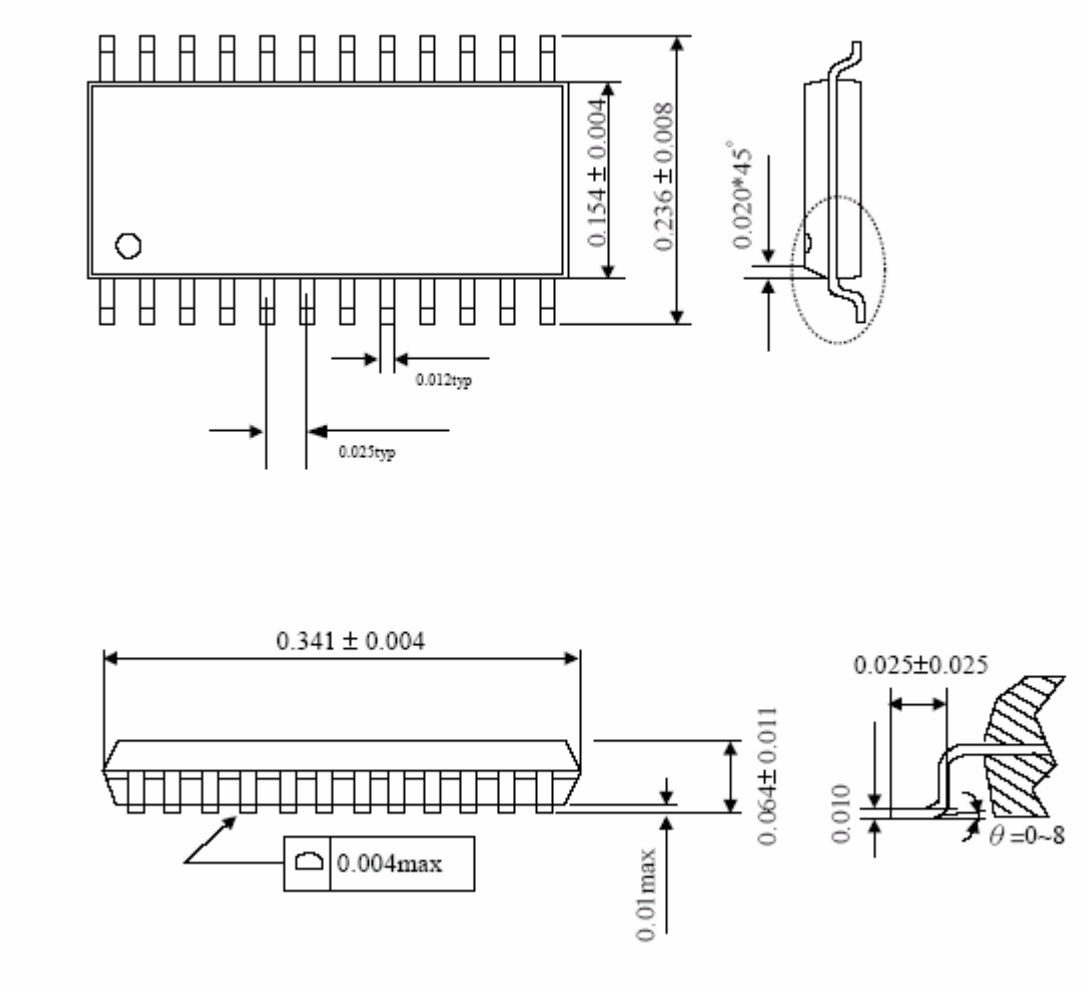
Package Outline Dimension

24 SKINNY PDIP(300)



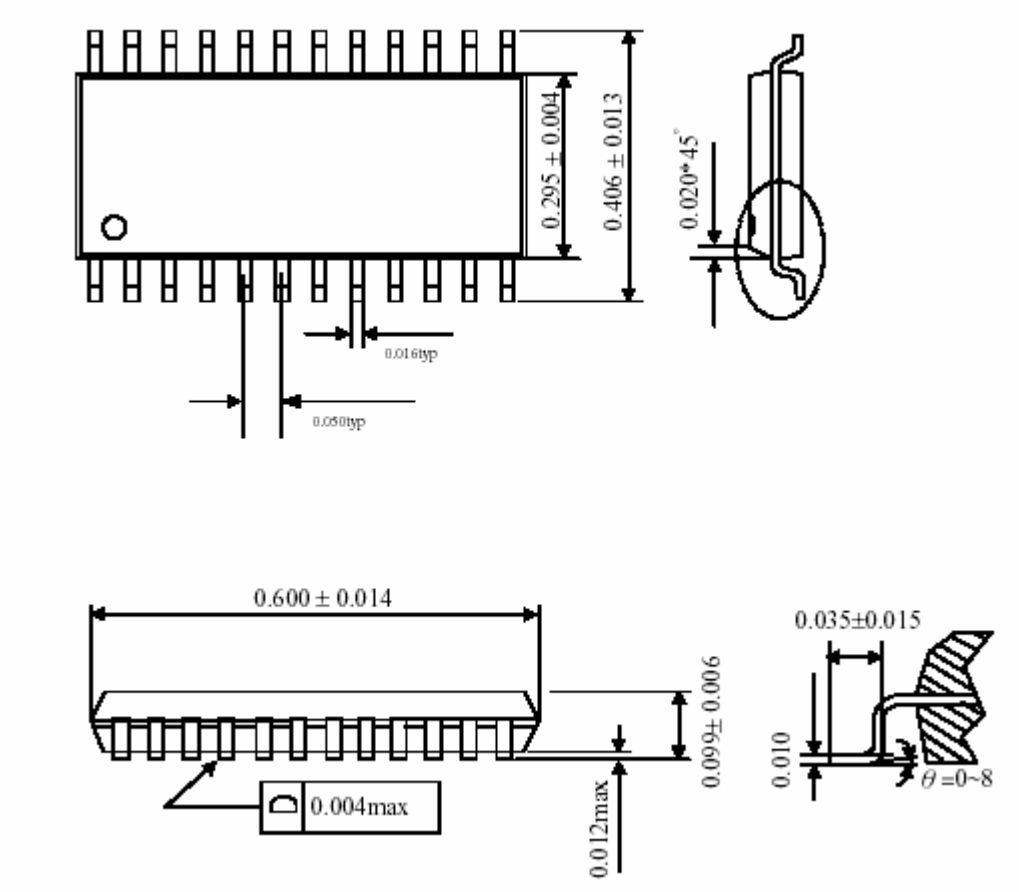
Package Outline Dimension

24SSOP(150mil, 0.64mm lead-pitch) **UNIT: INCH**



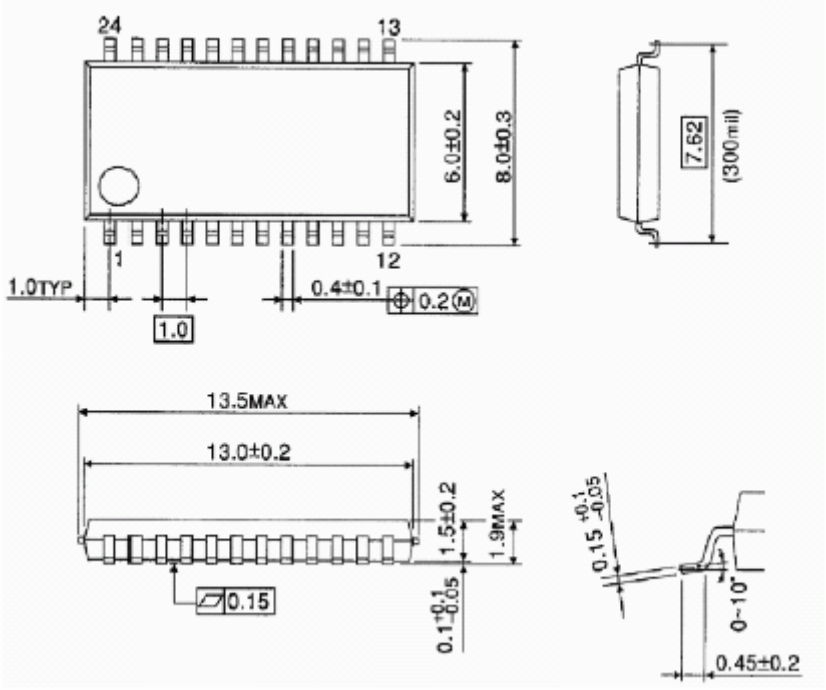
Package Outline Dimension

24SOP(300mil, 1.27mm lead-pitch) **UNIT: INCH**



Package Outline Dimension

24SSOP(300mil, 1.0mm lead-pitch) **UNIT: mm**



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